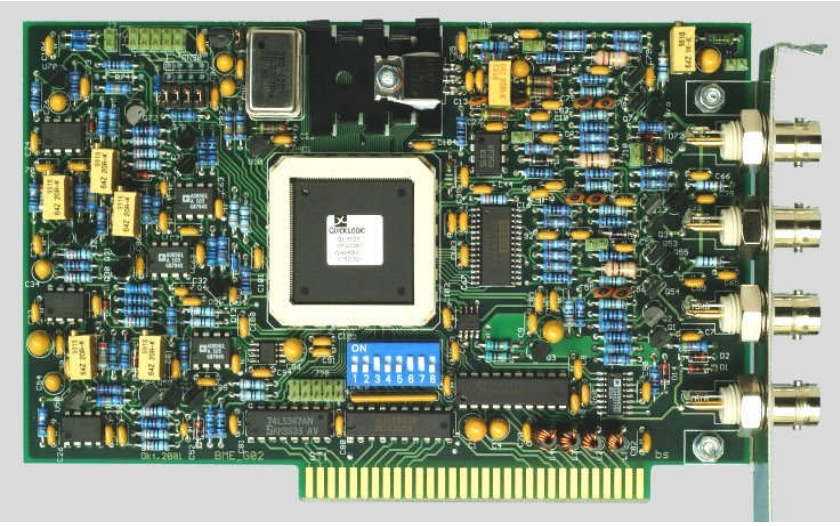
Digital Delay/Pulse Generator

Model BME_G02



- PC-ISA-Card
- 3 Delays(BNC Output), with 25ps Delay-Resolution and 44bit Delay-Range (max. Delaytime = 429s)
- Edge or Gate Output
- Master/Slave Option (if more than 3 Outputs are needed)
- high Load Option

Circuit Description

The BME_G02 is a PC-ISA card having 3 delay lines that can produce delayed signals from 50nsec to 419sec in steps of 25psec.
A trigger circuit starts the delay counters. There are 4 counters, T, A, B and an auxiliary counter. The T, A and B counters actually produce an output signal, while the auxiliary counter can only be used to produce an interrupt. In Edge-Mode the first level transition is dermined by the programmed Delay - after the last Delay expires all outputs are reset together. In Gate-Mode the outputs A and B can be combined to form a gate signal, i.e. a rising(falling) edge after delay A has elapsed and a falling(rising) edge after delay B has elapsed, so you get an pulse with a variable(25ps resolution) pulse-width from 2ns – 429s.
The trigger can be produced internally by a modulo-N counter or by an external signal. The external trigger can by used as external clock, and can additionally can be gated and prescaled.
If more than 3 Outputs (or more than 1 Gate output) are needed, two ore more card's can be connected together via a ribbon-cable, resulting in 6 or more synchronous delayed outputs.

Options:

BME_SG02:	Outputs synchronized to external trigger
BME_G03:	the outputs T, A, and B can individually be reset with a resolution of 100ns.
BME_G04:	these three outputs can be fired a second time before they are reset by a common reset signal.

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Specifications

Delays

Delayrange:		50ns – 429s (44bit)	
Delayresolution:		25ps	
min. Delaytime:		50ns (Insertion-Delay)	
Error:		<(1ns + 25ppm * delay)	**)[1]**
RMS Jitter:	Output to Output	<(50ps + 10^{-8} * delay)	**)[1]**
	Trigger to Output	<(50ns + 10^{-8} * delay)	
	Trigger to Output	<(300ps + 10^{-8} * delay)	) only BME_SG02

Trigger

External:		
	Threshold Range:	-2.5V to 2.5V in Steps of 1.2mV
	Slope:	rising or falling edge
	Input impedance:	10kΩ or 50Ω
Internal:		by a modulo-N counter running with the main clock

Outputs T,A,B

Mode:		Slope or Gate (AB) output	
Load:		50Ω or 25Ω,	
		T0 output can be configured for NIM output pulse	
Risetime:		<2ns for TTL	
		<1.2ns for ECL or NIM (typical)	
Levels:	TTL:	0 to 4V	normal or inverted
	ECL:	into -2.0V	normal or inverted
	NIM		

Interrupts

can be fired with the finish of any of the delays T, A, B, or after an auxiliary delay has finished. It is also possible to fire an interrupt with the main trigger of the delay generator(s), or after a fixed number of triggers has occurred.
An Interrupt can be requested on lines int3 , int4,.... int7 of the PC XT/AT bus.

General

Clock Source:	Internal:	10Mhz (80MHz) 25ppm	**)[1]**
	External:	max. 250MHz with prescaler	
Master/Slave option set by jumper			
Interface:		PC XT/AT bus (ISA 8bit)	
		I/O adressable between 000 and 3F0 H	
Dimensions:		PC-Board 170x110 mm	

Software

C Library
Labview DLL
Standalone Control Program

)[1] Accuracy and Jitter depend on clock source (specs with 25ppm clock source) optional 1ppm clock source available

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