Digital Delay/Pulse Generator

Model BME_SG02p

- PCI-Card
- 3 Delays(SMA Output), with 25ps Delay-Resolution and 44bit Delay-Range (max. Delaytime = 429s)
- very low Jitter
- max. Repetition Rate 8MHz
- Edge, Gate or Pulse Output
- Master/Slave Option (if more than 3 Outputs are needed)
- high Load Option
- several output voltage levels
- external/internal (modulo-N counter) Trigger
- external/internal clock

Options:

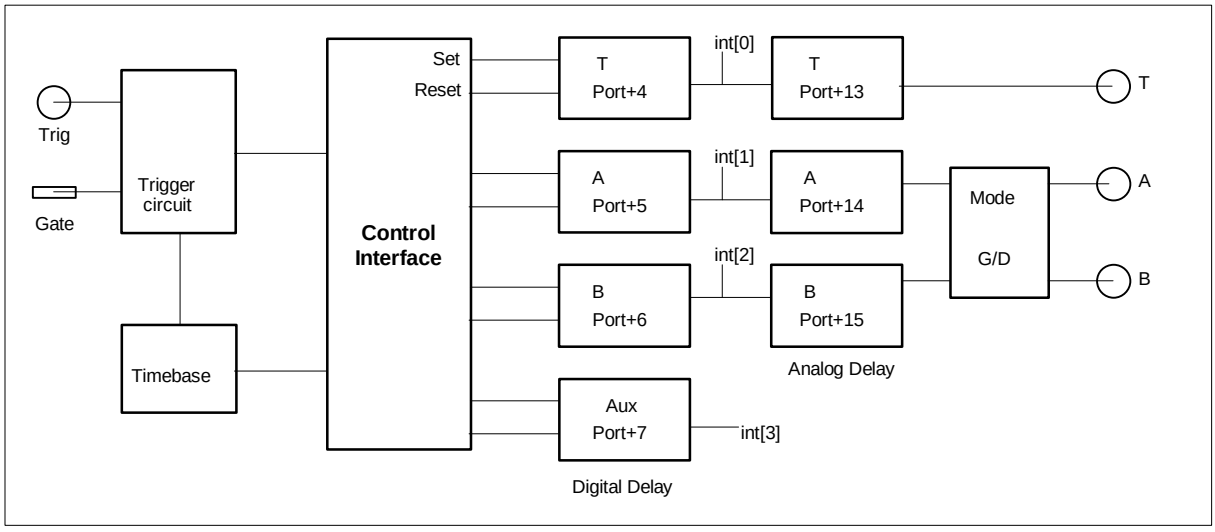
BME_SG02p:	Outputs synchronized to external trigger
BME_G03p:	the outputs T, A, and B can individually be reset with a resolution of 100ns.
BME_G04p:	these three outputs can be fired a second time before they are reset by a common reset signal.
BME_G05p:	the ouputs can be vetoed with a modulo-counter

BME KG Hagener Leite 24 D-82418 Murnau Germany Tel +49-(0)8841 487769 1
Fax +49-(0)8841 487769 9 e-mail bme-bergmann@t-online.de http://www.bme-bergmann.de

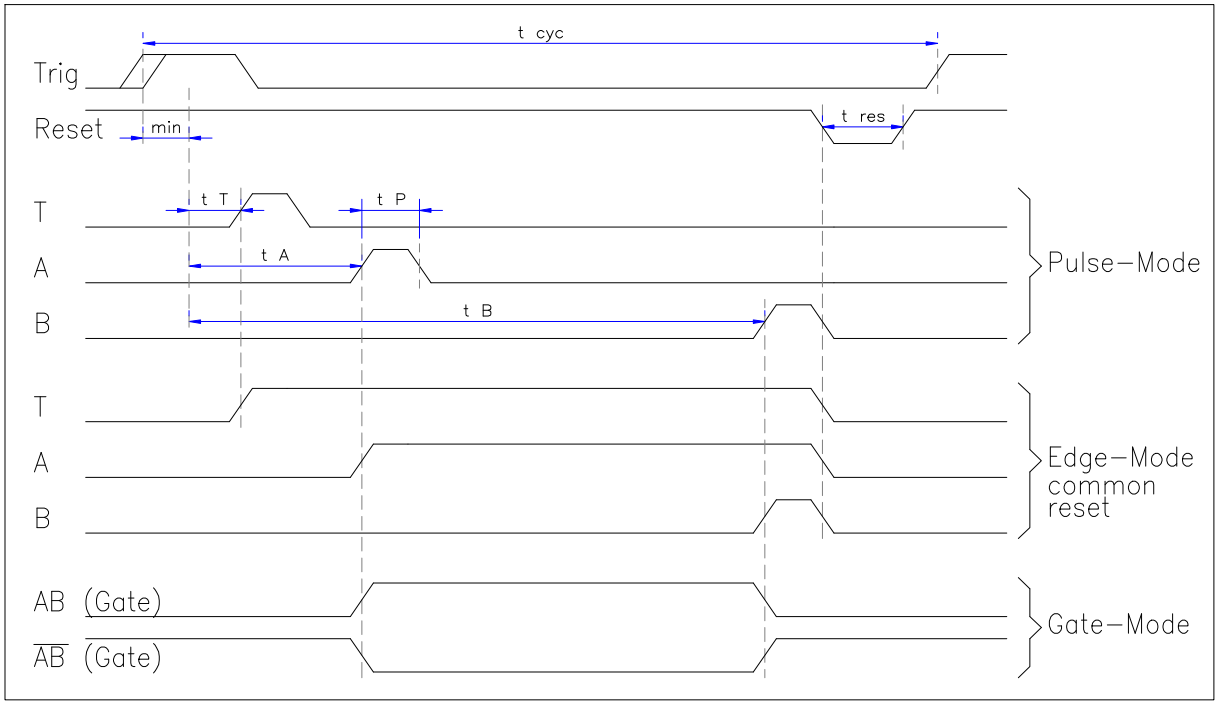
Circuit Description

The BME_G02p is a PCI card having 3 delay lines that can produce delayed signals from 50nsec to 419sec in steps of 25psec.
A trigger circuit starts the delay counters. There are 4 counters, T, A, B and an auxiliary counter. The T, A and B counters actually produce an output signal, while the auxiliary counter can only be used to produce an interrupt. In Pulse-Mode each programmed delay produces a pulse of specified length at its output connector, in Edge-Mode the first level transition is determined by the first programmed Delay - after the last Delay expires all outputs are reset together. In Gate-Mode the outputs A and B can be combined to form a gate signal, i.e. a rising(falling) edge after delay A has elapsed and a falling(rising) edge after delay B has elapsed, so you get an pulse with a variable(25ps resolution) pulsewidth from 2ns – 429s.
The trigger can be produced internally by a modulo-N counter or by an external signal. The signal connected to the external trigger input can also be used as external clock, and can additionally can be gated and prescaled.
If more than 3 Outputs (or more than 1 Gate output) are needed, two ore more cards can be connected together via a ribbon-cable, resulting in 6 or more synchronous delayed outputs.

Blockdiagram



Timing



Specifications

Delays

Delayrange:		50ns – 429s (44bit)	
Delayresolution:		25ps	
min. Delaytime:		50ns (Insertion-Delay)	
Error:		<(1ns + 25ppm * delay)	)[2]
RMS Jitter:	Output to Output	<(50ps + 10^{-8} * delay)	)[2]
	Trigger to Output	<(50ns + 10^{-8} * delay)	
	Trigger to Output	<(250ps + 10^{-8} * delay)	) only BME_SG02

Trigger

External:	Threshold Range:	-2.5V to 2.5V in Steps of 1.2mV
	Slope:	rising or falling edge
	Input impedance:	10kΩ or 50Ω
Internal:		by a modulo-N counter running with the main clock
	Repetition rate:	from 0.002Hz to 8MHz

Outputs T,A,B

Mode:		Edge, Pulse or Gate (AB) output	
Load:		50Ω or 25Ω,	
		T0 output can be configured for NIM output pulse	
Risetime:		<2.3ns for TTL	
		<1.5ns for ECL or NIM (typical)	
Levels:	TTL:	0 to 4V)[1]	normal or inverted
	ECL:	into -2.0V	normal or inverted
	NIM		

Interrupts

can be fired with the finish of any of the delays T, A, B, or after an auxiliary delay has finished. It is also possible to fire an interrupt with the main trigger of the delay generator(s), or after a fixed number of triggers has occurred.

General

Clock Source:	Internal:	10Mhz (80MHz)	)[2]
		Accuracy: 25ppm(0-70°C); T.C.: <1ppm/°C	
	External:	max. 250Mhz with prescaler	
Master/Slave option set by jumper			
Interface:		PCI bus	
		signal compatibility 3.3V and 5V	
Dimensions:		PC-Board 170x110 mm	

Software

C Library
Labview DLL
Standalone Control Program

)[1] 5V amplitude available as an option
)[2] Accuracy and Jitter depend on clock source (specs with 25ppm clock source)
optional 1ppm clock source available

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Application: Jitter-Free Control of a Femtosecond Lasersystem

shown below is typical example of a fs-laser system, an oscillator with two amplifiers, the first stage running at 10Hz, the second stage running at 1Hz. This demonstration has been derived from a diode pumped fs laser system built at the university of Jena, Germany.

A photodiode picks up the oscillator 76MHz signal which is fed into the external clock/trigger input of a BME_SG02 card. Using the fs-oscillator as the external clock 7 separately delayed outputs have to be fired synchronously to the arriving laser pulses with an allowed jitter of less than 0.5ns (actuallly the jitter is in this case only 50psec) and the output voltages fitted to specific needs of various devices.

The BME_SG02 master card sets the base repetition frequency of 10Hz. The BME_G05 slave cards have an output scaler that divides down the base repetition frequency of 10Hz by any integer number, in this case dividing it by 10 to get a repetition frequency of 1 Hz for the second amplifier. Thus it is possible to run the first amplifier at a repetition rate of 10Hz and the second at 1Hz without any additional device as well as exactly triggering further Pockels cells, pump lasers and instrumentation.

The timing of the laser system is as follows:

a) Since the pumplaser of the 2. amplifier is a laser diode stack, it must be fired roughly 2msec before the laser pulse
b) The flashlamp of the 1. amplifiers pumplaser must be fired 180usec in advance
c) the Q-switch of the 1. amplifiers pumplaser must be fired 3usec in advance
d) the timing of the pockels cells comes with the laser pulse and must be completely jitterfree for optimum performance of the laser system

As an option, it is possible to use the 50Hz line signal to derive the 10Hz base repetition rate of the laser system. Synchronizing the 10Hz base repetition rate of the laser system to the 50Hz line frequency might be advantageous, if line voltage variations can effect the output stability of the laser system.

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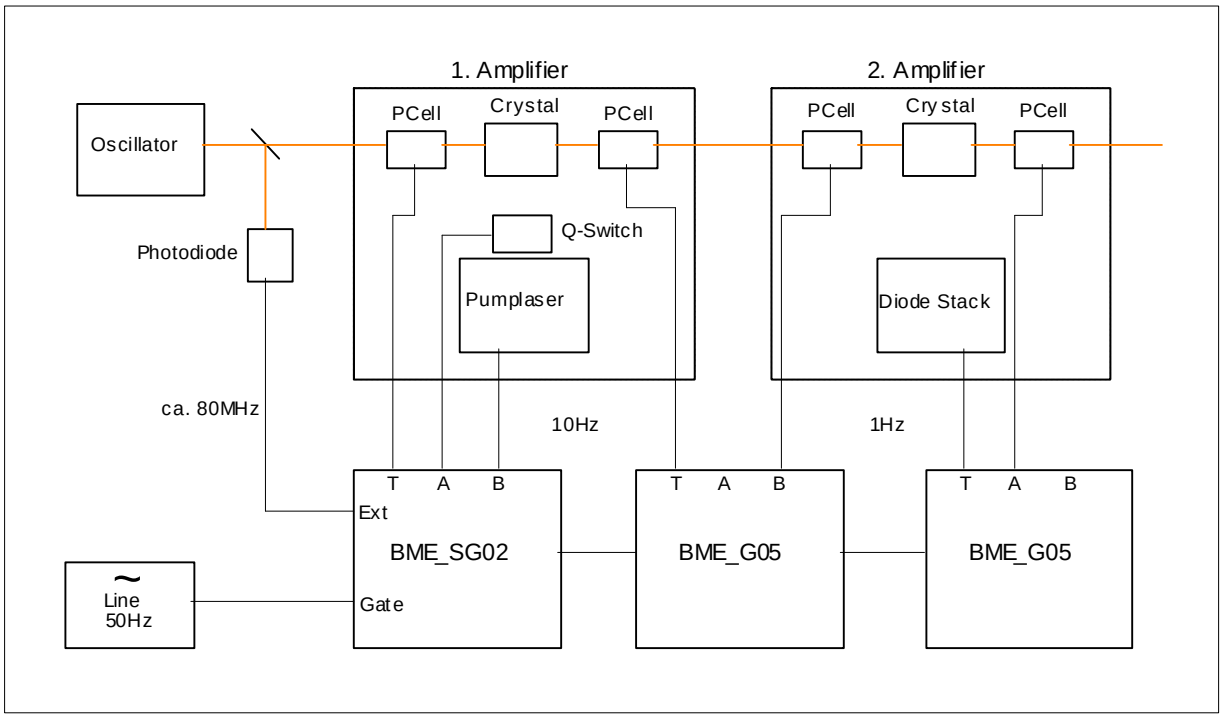

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